

Fourth Semester B.E. Degree Examination, Dec.2015/Jan.2016

Fundamentals of HDL

Time: 3 hrs.

Max. Marks:100

Note: Answer FIVE full questions, selecting at least TWO questions from each part.

PART – A

- 1 a. Explain VHDL data types with an example for each. (10 Marks)
- b. If $A = 110$, $B = 111$, $C = 011000$ and $D = 111011$. Verify $(A \text{ and not } B \text{ or } C \text{ xor } 2 \text{ and } D) = 110010$. True or False. (05 Marks)
- c. Write a verilog description of the following combinational network using concurrent statements. Each gate has a 5 ns delay, excluding the inverter, which has a 2-ns delay.

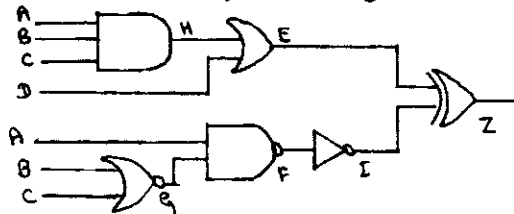


Fig.Q1(c)

(05 Marks)

- 2 a. Write a VHDL 2×2 unsigned combinational array multiplier. (06 Marks)
- b. With the help of a truth table, logic diagram and logic symbol, write a HDL description of 2×1 multiplexer with active low enable. (10 Marks)
- c. Explain constant declaration and assignment statement with example. (04 Marks)
- 3 a. Explain various loop statements in HDL with examples. (12 Marks)
- b. Write a VHDL 4-bit counter with synchronous clear description. (08 Marks)
- 4 a. Write a HDL structural description of a pulse-triggered, Master-slave D flipflop. (12 Marks)
- b. Write a VHDL N-bit asynchronous down counter using generate statement. (08 Marks)

PART – B

- 5 a. Explain task with syntax and write a verilog N-bit ripple-carry adder using task. (10 Marks)
- b. Explain procedure with syntax and write a VHDL code for converting a fraction binary to real using procedure. (10 Marks)
- 6 a. Describe all file processing tasks in verilog with examples. (08 Marks)
- b. Write the block diagram and function table of a SRAM. Using these, write a VHDL description for 16×8 SRAM. (12 Marks)
- 7 a. How to invoke a VHDL entity from a verilog module? (08 Marks)
- b. Write a mixed language description of 3-bit synchronous counter with clear to show how a verilog module invoke from a VHDL module. (12 Marks)
- 8 a. Describe synthesis information from entity and module with examples. (10 Marks)
- b. Write the steps for synthesis. (05 Marks)
- c. Explain mapping the if statement to gate-level with suitable example. (05 Marks)